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(51) INT CL⁴
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(52) Domestic classification
B1S 102 FB FDH13 FDJ10
U1S 1421 B1S

(56) Documents cited
GB A 2142346 GB 1029663 US 4323417
GB 1037909 GB 0998723

(58) Field of search
B1S

(54) Semiconductor device and process for making it

(57) Seed crystals are made in a region of a polycrystalline layer on a substrate by melting the region and then cooling it so that it solidifies from one end to the other in a first direction and outwardly toward the edges in a second direction normal to the first direction. The desired cooling pattern is established by providing a thermal layer under the polycrystalline layer, which thermal layer is used to provide different rates of heat conduction therethrough in different parts of the thermal layer. A large, single-crystal device can be made by providing an operating layer of polycrystalline material in contact with the seed, melting the operating layer and recrystallizing it so that its solidification proceeds from the seed. The thermal layer can be used to enhance the desired direction of resolidification by providing different rates of heat conduction therethrough in different parts of the thermal layer.

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FIG. 1

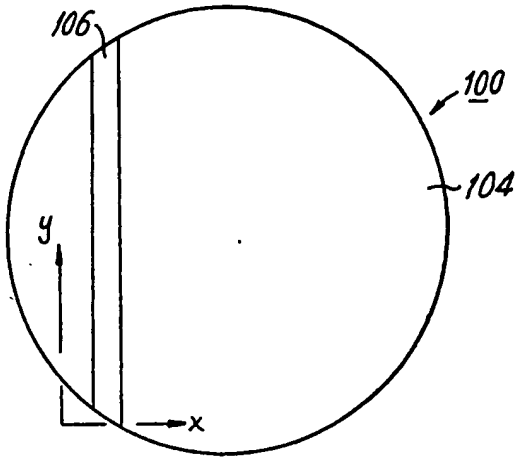
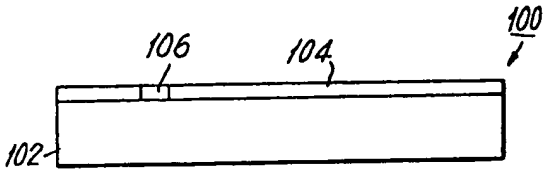


FIG. 2



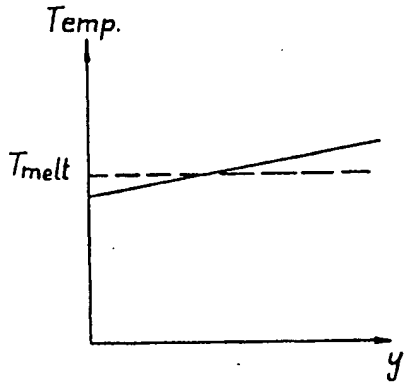


FIG. 3

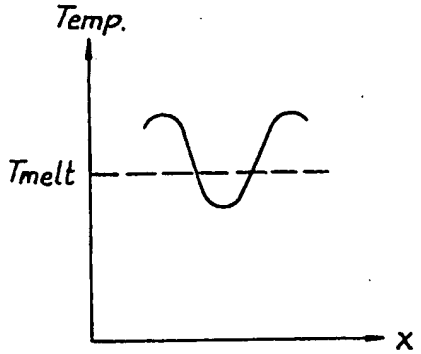


FIG. 4

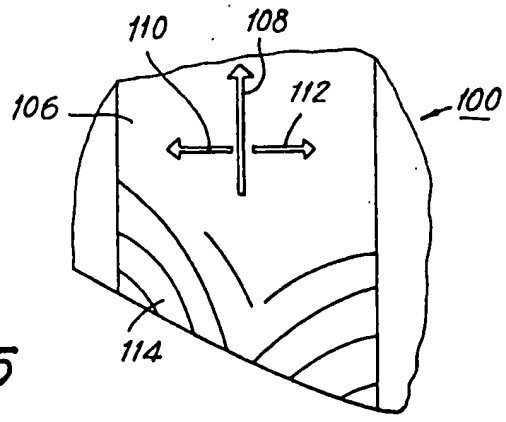


FIG. 5

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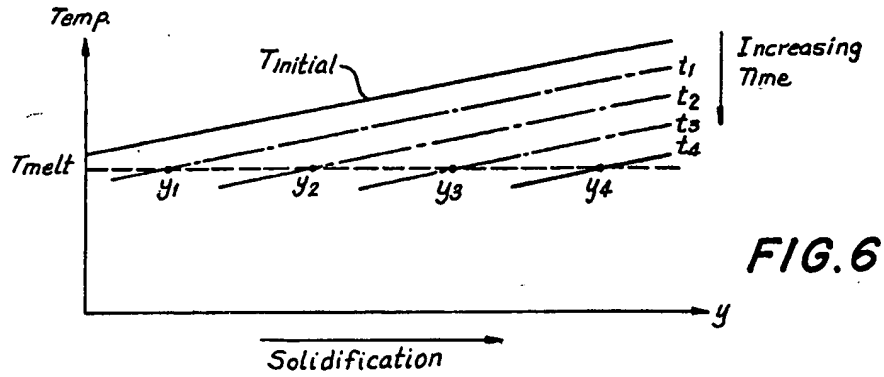

FIG. 6

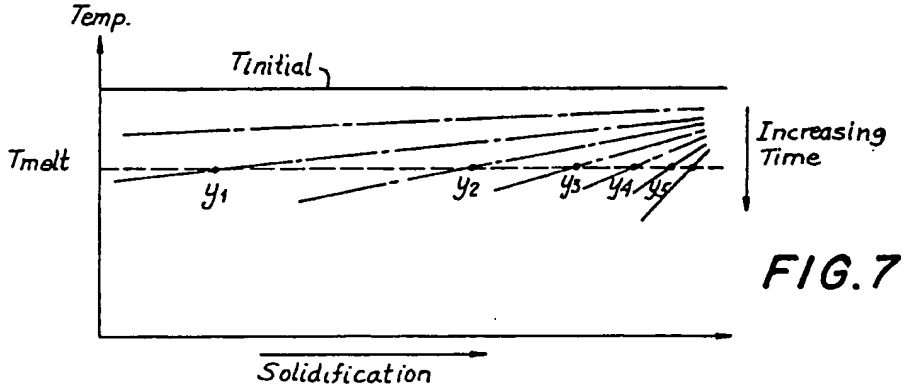

FIG. 7

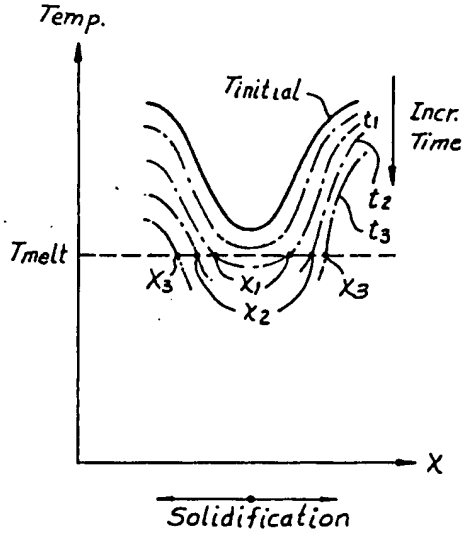

FIG. 8

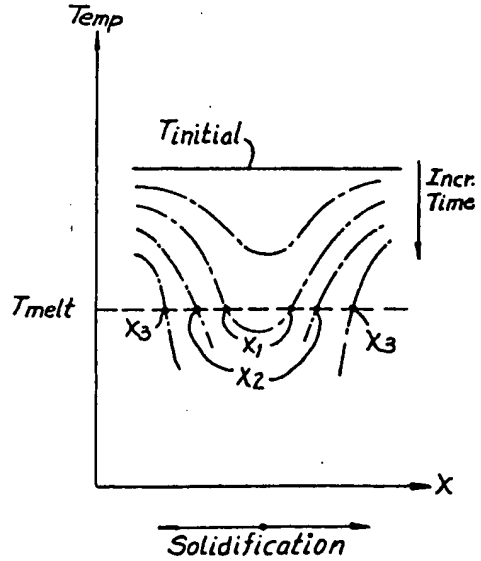

FIG. 9

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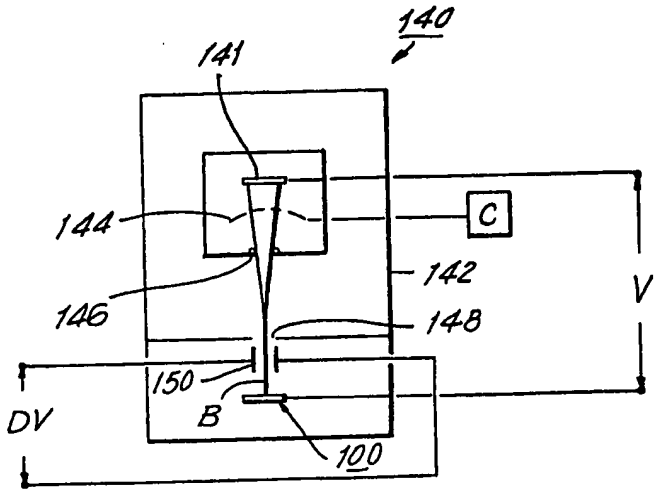

FIG. 10

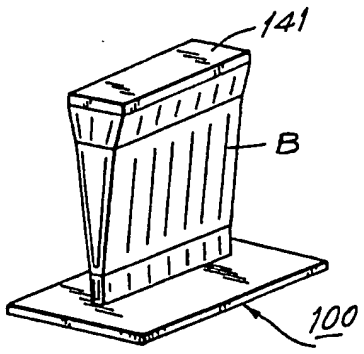

FIG. 11

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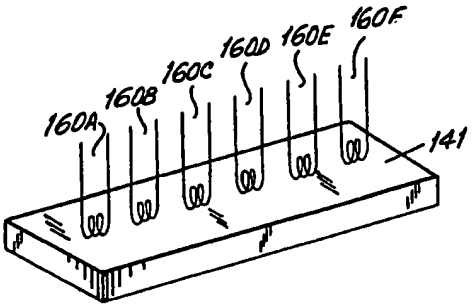
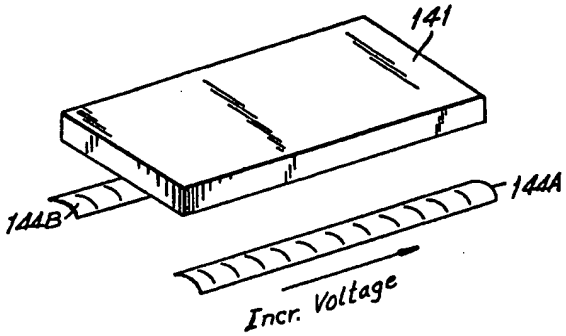


FIG. 12

FIG. 13



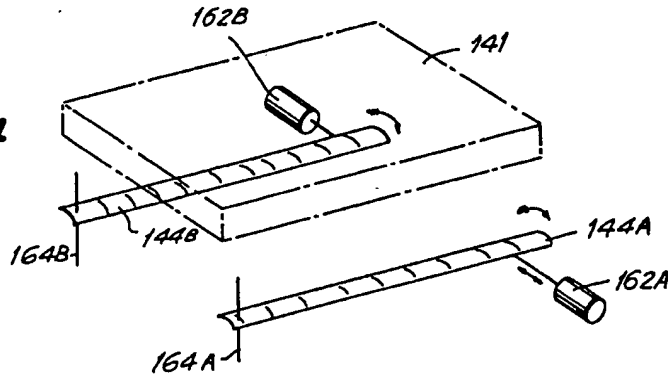


FIG. 14

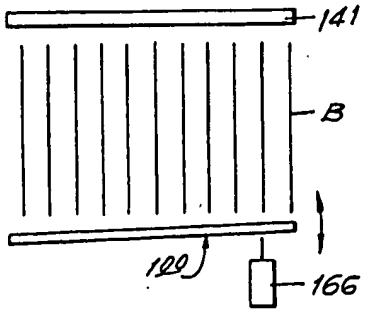


FIG. 15

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FIG.16

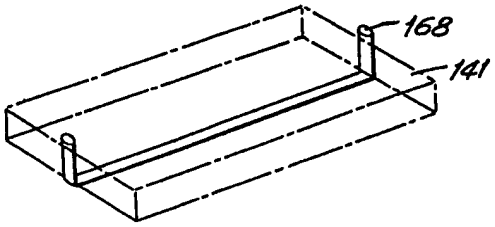
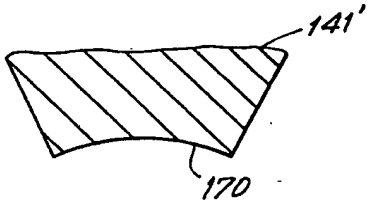


FIG.17

FIG.18



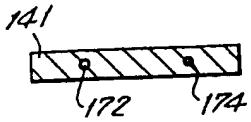
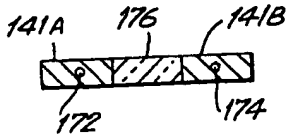


FIG.19



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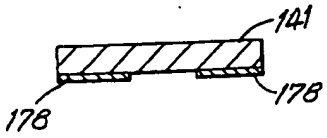

FIG.21

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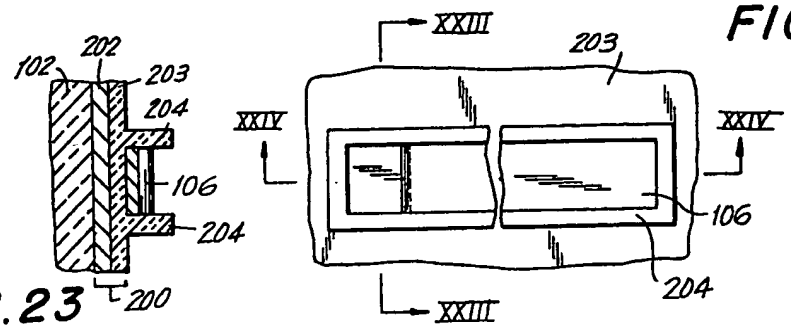

FIG. 22

FIG. 23

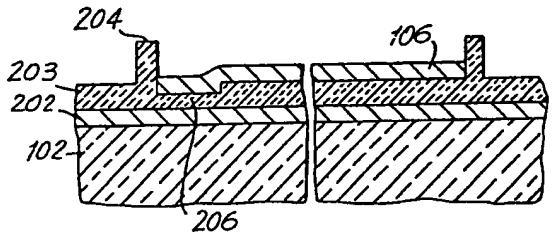

FIG. 24

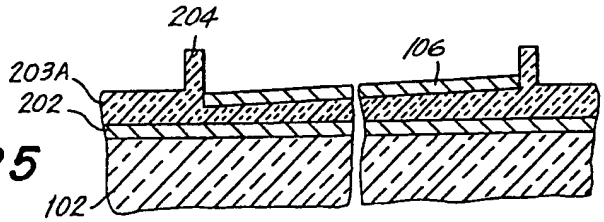

FIG. 25

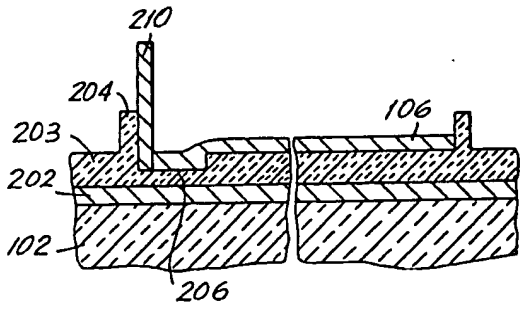

FIG. 26

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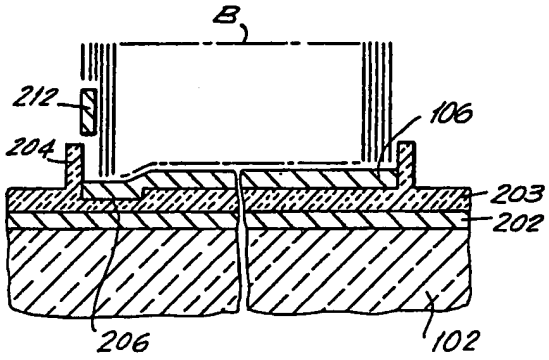

FIG. 27

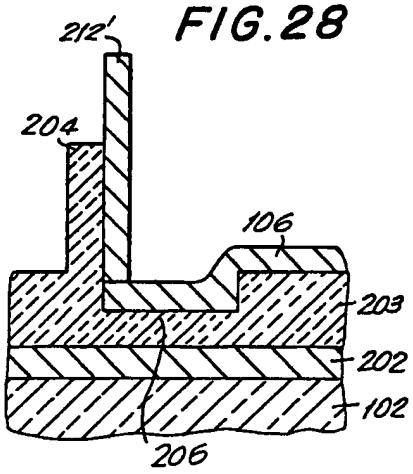

FIG. 28

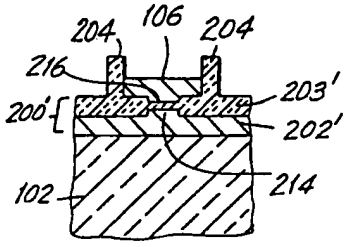

FIG. 29

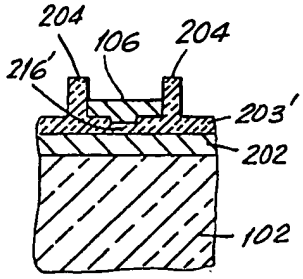

FIG. 30

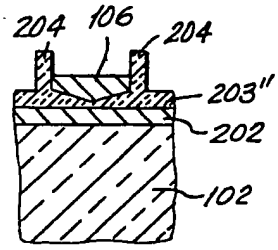

FIG. 31

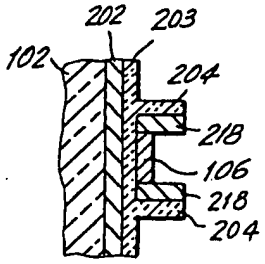

FIG. 32

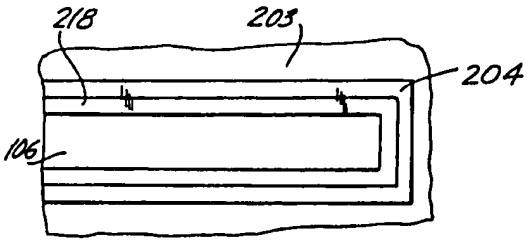

FIG. 33

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FIG.34

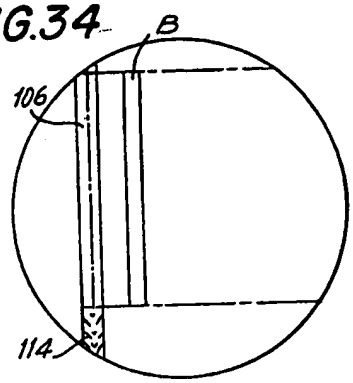
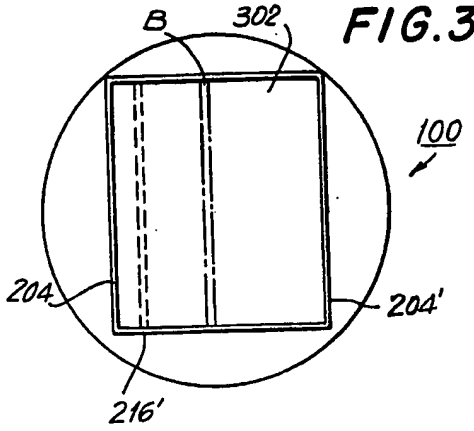


FIG.39



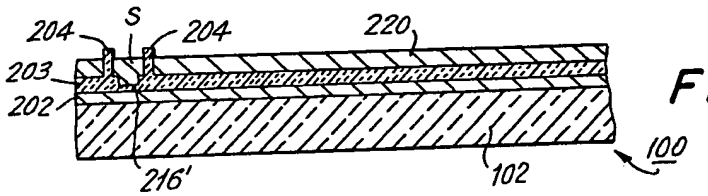


FIG.35

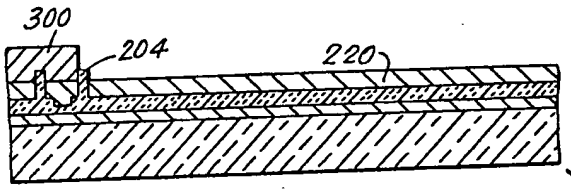


FIG.36

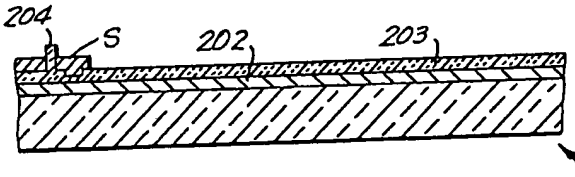


FIG.37

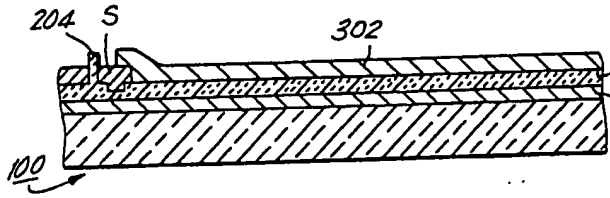


FIG.38

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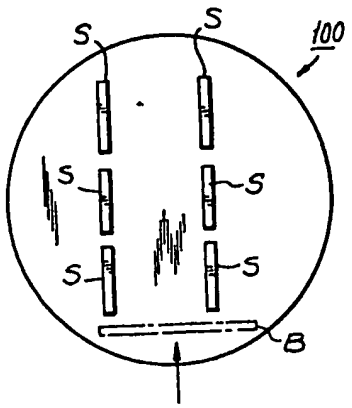

FIG.40

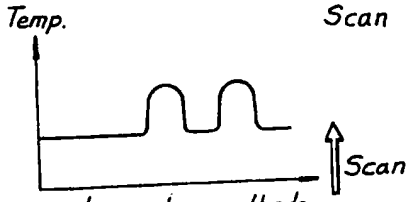

FIG.41

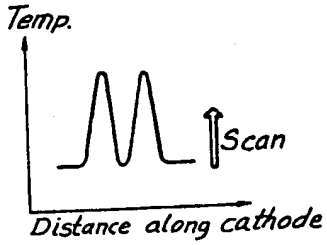

FIG.42

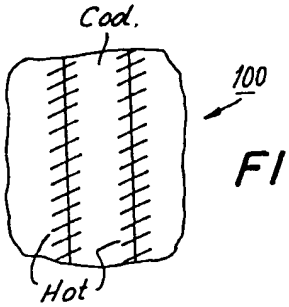

FIG.43

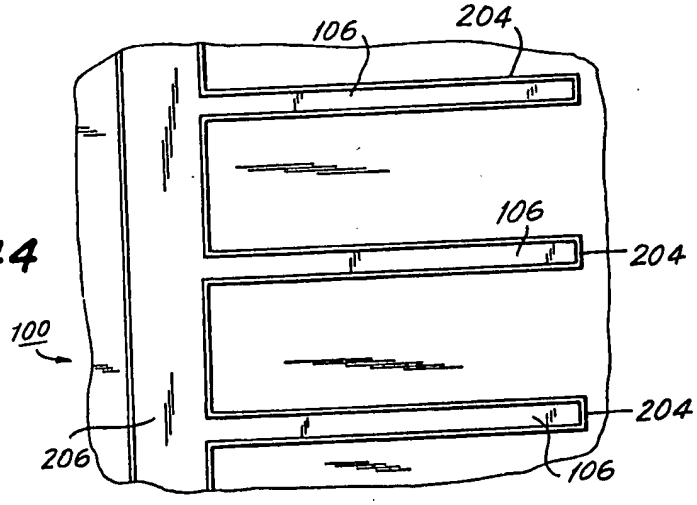

FIG.44

SPECIFICATION

Wafer construction for making single crystal semiconductor device

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor devices and, more particularly, to large, single-crystal semiconductor devices and wafer constructions for producing such devices.

Description of the Prior Art

The use of a high-energy beam for growing a large single crystal from a layer of polycrystalline material on a substrate has been proposed. As the beam scans the substrate it melts the layer and, ideally, when the molten zone cools it solidifies into a single crystal.

One of the conditions required to convert the polycrystalline layer into a single crystal is the provision of a "seed", that is, a single crystal which is in contact with the molten zone to cause it to solidify as a single crystal. There has not yet been proposed any completely satisfactory means of producing such a seed.

Various conventional energy sources, such as a spot laser beam, spot electron beam, graphic strip heater and arc strip lamp, have been proposed for use in melting the polycrystalline layer to induce liquid or solid phase regrowth by epitaxial recrystallization.

However, such conventional energy sources are unsatisfactory. For example, spot beam energy sources produce a resulting recrystallized layer lacking a uniform single-crystalline structure. Conventional strip beam energy sources, such as graphite strip heaters and arc strip lamps, can damage the underlying substrate because they require a relatively long time of contact of the beam with the polycrystalline layer, which results in dissipation of an unacceptable amount of heat from the layer into the underlying substrate.

Such energy sources are also unsuitable for producing a single seed crystal. A spot laser or electron beam, impinging momentarily on a polycrystalline layer, will create a relatively small, circular molten region in the layer. However, when the region solidifies, its boundary with the rest of the layer contains small silicon crystals, which of course make the region unsuitable for use as a seed. Scanning the layer with a spot beam has also not provided a suitable seed. And the conventional strip energy sources are unsatisfactory for the same reason that they cannot be used for growing a single-crystal layer.

SUMMARY OF THE INVENTION

It is an object of the present to invention provide a wafer construction for use in forming a single-crystal semiconductor device that overcomes the shortcomings of the prior art.

It is an object of the present invention to provide a wafer comprising a substrate and a polycrystalline or amorphous layer thereon having a region which, when melted, solidifies as a single crystal for use as a seed for making a large, single-crystal semiconductor device.

It is another object of the present invention to provide a wafer comprising a substrate and single-crystal seed and a polycrystalline or amorphous layer on the substrate which, when melted, solidifies as a single crystal.

In accordance with an aspect of the invention a wafer comprises a substrate, a thermal layer on the substrate and a polycrystalline or amorphous seed layer on a region of the thermal layer. The thermal layer provides different rates of heat conduction therethorugh in at least one of a first direction of the region or a second direction substantially normal to the first direction, wherein the rate of heat conduction through said thermal layer in said first direction provides an increasing temperature gradient in the seed layer in the first direction and the rate of heat conduction through the thermal layer in the second direction provides a higher temperature at the edges of the region than centrally thereof in the second direction.

In accordance with another aspect of the invention, a wafer comprises a substrate, a thermal layer on the substrate, a single-crystal seed on the thermal layer and extending in a first direction and a polycrystalline or amorphous layer on the thermal layer covering an area bounded on one side by the seed and extending in a second direction away from the seed and normal to the first direction. The polycrystalline or amorphous layer is in contact with the seed and the thermal layer provides different rates of heat conduction through the thermal layer in the second direction for creating an increasing temperature gradient in the polycrystalline or amorphous layer in the second direction.

Those and other objects, features and advantages of the present invention will become apparent when the following detailed description of preferred embodiments of the invention is considered with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a top view of a wafer schematically illustrating in principle the provision of a region in which a seed crystal is formed in a polycrystalline or amorphous layer on a substrate.

Figure 2 is a side elevation view of the wafer shown in Fig. 1.

Figure 3 is a plot of the temperature gradient in the region shown in Fig. 1 in a first direction at any given time during the resolidification of the region after it has been melted.

Figure 4 is a plot of the temperature gradi-

ent in the region shown in Fig. 1 in a second direction at any given time during the resolidification of the region after it has been melted.

Figure 5 shows the directions of resolidification of the molten region.

Figure 6 illustrates one temperature gradient over time in the region shown in Fig. 1 in the first direction.

Figure 7 illustrates another temperature gradient over time in the region shown in Fig. 1 in the first direction.

Figure 8 illustrates one temperature gradient over time in the region shown in Fig. 1 in the second direction.

Figure 9 illustrates another temperature gradient over time in the region shown in Fig. 1 in the second direction.

Figures 10 and 11 illustrate apparatus for providing a strip-like electon beam for melting the region shown in Fig. 1.

Figures 12–15 illustrate apparatus for providing the initial temperature gradient shown in Fig. 6.

Figures 16–21 illustrate apparatus for providing the initial temperature gradient shown in Fig. 8.

Figures 22–28 illustrate wafer constructions for providing the temperature-time relationship shown in Fig. 7.

Figures 29–31 illustrate wafer constructions for providing the temperature-time relationship shown in Fig. 9.

Figures 32–33 illustrate an alternate embodiment of the wafer constructions shown in Figs. 22–31.

Figures 34–38 illustrate a method of making a single-crystal semiconductor layer using the seed formed on the wafer shown in Fig. 30.

Figure 39 illustrates a wafer construction for making a single-crystal semiconductor layer.

Figure 40 is a top view of a wafer like that shown in Fig. 1 with a plurality of seeds formed thereon.

Figure 41 illustrates a possible temperature profile in the polycrystalline layer of a wafer like that shown in Fig. 1.

Figure 42 illustrates another possible temperature profile in the polycrystalline layer of a wafer like that shown in Fig. 1.

Figure 43 is a top view of part of a wafer like that shown in Fig. 1 showing the temperature distribution created in the seed region by the embodiments shown in Figs. 41–42.

Figure 44 is a top view of an alternate wafer construction for making a plurality of single-crystal seeds.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figs. 1 and 2 show a wafer 100 from the top and in elevation, respectively. The wafer 100 comprises a circular substrate 102 about 3 inches in diameter having a layer 104 of polycrystalline or amorphous material on it about 0.5 to 1.0 micron thick. By "polycrystalline" is meant a material comprising a large number of relatively small crystals. A typical example is polysilicon, which will be used herein to describe the present invention. However, by using polysilicon to describe the features of the present invention it is not intended to limit the kinds of materials suitable for use as the polycrystalline or amorphous layer 104.

The layer 104 of polysilicon is deposited on the subtrate 102 by a method such as chemical vapour deposition ("CVD"). In the present invention, the substrate 102 can be any almost any material that presents a smooth surface, a feature which forms one of the advantages of the present invention, as will be appreciated from this description. Examples of materials suitable as a base for the substrate 102 are glass, quartz, sapphire and crystalline semiconductor materials such as silicon, germanium or gallium arsenide. The base can also be a single-crystal semiconductor material with semiconductor-device regions formed therein. The use of such a base is particularly advantageous because the present invention will enable a three-dimensional device to be constructed on the base. In any case, the polysilicon layer 104 is to be deposited on an underlying insulating layer, so that if the base of the substrate 102 is not an insulating material, then a layer (not shown in Fig. 1) of an insulating material such as SiO_2 or silicon nitride is used underneath the layer 104.

A seed comprising a single crystal of silicon is formed in the layer 104 of polysilicon by heating a region 106 of the layer 104 of polysilicon to above its melting point and then cooling the molten region under controlled conditions. Those conditions can be defined by establishing a coordinate system having "x" and "y" axes as shown in Fig. 1. To form a single-crystal seed the region 106 of polysilicon is heated to above the melting point of silicon, for example, to about 1400°C, and then cooled to establish the temperature gradients shown in Figs. 3 and 4 at any particular time during cooling. "T_{melt}" indicates the melting point of silicon. At any given time the temperature gradient (in °C per cm) across the solid-liquid interface in a given direction in the solidifying region should have a minimum value which depends in the solidification speed in that direction and the material. For example, for polysilicon, the temperature gradient in °C per centimeter should be at least 5000 times the solidification speed in centimeters per second.

Fig. 5 illustrates how those temperature gradients create a single crystal from the molten region 106. As the region 106 cools, the molten silicon solidifies in the directions shown by the arrows 108, 110 and 112. Solidification of the region 106 proceeds

along a first direction shown by the arrow 108 and outwardly toward the edges, as shown by the arrows 110 and 112, in a second direction normal to the first direction. This cooling pattern converts virtually the entire region 106 into a single crystal, with the exception of a small portion 114 at one end.

Figs. 6–9 illustrate how that cooling pattern can be created. Figs. 6 and 7 show the creation of a temperture distribution in the first direction (that is, in the y-direction as seen in Fig. 1).

In the embodiment illustrated in Fig. 6, the region 106 is initially heated so that it exhibits the increasing temperature gradient shown in Fig. 6. The region 106 then cools uniformly along its length (in the y-direction) and, as each location in the region 106 cools below the melting point of silicon, it solidifies. At time t_1, for example, the region 106 at y_1 solidifies; at time t_2, the region 106 at y_2 solidifies, and so on. Thus, the region 106 solidifies in the direction of the arrow 108 in Fig. 5.

Alternatively, the region 106 can initially be heated to a uniform temperature as shown in Fig. 7. In this embodiment the temperature distribution is established as the region 106 cools. The solidification direction is established by the non-uniform cooling pattern graphically illustrated in Fig. 7, in which the locations y_1, y_2, y_3, etc., solidify at times t_1, t_2, t_3, etc., respectively, similar to the embodiment shown in Fig. 6.

Figs. 8 and 9 show how the proper temperature distribution can be established across the region 106 in the second direction (that is, along the x-axis). As shown in Fig. 8, the region 106 can be initially heated to establish the temperature gradient shown as $T_{initial}$. Then, as the zone 106 cools, the locations x_1, x_2 and x_3 solidify at times t_1, t_2 and t_3, respectively. Hence, the direction of solidification, as shown graphically in Fig. 8, is in the direction of the arrows 110 and 112 in Fig. 5.

Alternatively, the region 106 can be initially heated to a uniform temperture as shown in Fig. 9, and then cooled non-uniformly. In that case, solidification proceeds as is graphically shown in Fig. 9, which also corresponds to the direction of the arrows 110 and 112 in Fig. 5.

The creation of a molten region in the layer 104 requires the deposit of a large amount of energy in the layer. That can be accomplished by using the fine-line electron beam disclosed in co-pending United States Patent Application Serial No. 455,266, filed on January 3, 1983, as a continuation of Patent Application Serial No. 224,313, and assigned to the assignee of the present invention.

As disclosed in that application, such an electron beam can be generated using the apparatus 140 shown in Figs. 10 and 11. The apparatus 140 creates a strip electron beam B that can deposit electrons with kinetic energies, power densities and energy densities having levels which melt a surface region of a workpiece, here the wafer 100, quickly enough to prevent heat conduction to the substrate underlying the surface region.

The apparatus 140 consists of a strip-like thermionic cathode 141 which is disposed in an evacuated housing 142 and is heated to release electrons. An extraction grid 144 controls the electrons and injects them to a focussing aperture 146. The electrons then pass through a ground aperture 148. A deflection system comprises electrostatic plates 150 across which a deflection voltage DV is applied. A potential difference V is maintained between the substrate 100 and the cathode 141 and a control system C can be provided to control the extraction grid voltage.

Fig. 11 shows schematically the shape of the electron beam B.

In this embodiment the electron beam B momentarily impinges, for between 10 and 1000 microseconds, on the layer 104 initially to melt the entire region 106, which is then left to cool and solidify as described above in connection with Figs. 6–9.

Figs. 12–15 illustrate embodiments in which the region 106 is initially heated with the proper temperature gradient in the y- or first direction, as described above in connection with Fig. 6.

In Fig. 12 the cathode 141 is heated non-uniformly along its length by a plurality of resistance heaters 160A, 160B, 160C, 160D, 160E and 160F. If the current supplied to each heater is slightly larger than that supplied to the immediately preceeding heater, then the current density of the beam B varies along the y-axis and the region 106 is heated non-uniformly along its length.

In Fig. 13 the cathode 141 is heated uniformly along its length, but the extraction grid elements 144A and 144B have applied thereto a potential gradient in the first direction. Thus the electron beam B has a higher current density at one end and heats the region 106 with the temperature gradient shown in Fig. 6.

In Fig. 14 the cathode 141 is heated uniformly along its length and the extraction grid elements 144A and 144B have a uniform potential along their length. However, motors 162A and 162B are used to vary the distance between the elements 144A and 144B by rotating the elements about axes 164A and 164B, respectively. Again, the effect is to provide an initial temperature gradient like that in Fig. 6 in the region 106.

Fig. 15 shows another embodiment in which the cathode C is uniformly heated. A motor 166 is used to change the angular orientation of the wafer 100 relative to the

cathode 141 to create the temperature gradient shown in Fig. 6.

Figs. 16–21 illustrate embodiments by which the region 106 can be initially heated with the lateral temperature distribution in the x- or second direction described above in connection with Fig. 8.

In Fig. 16, a conductive element 168 is placed underneath the cathode 141 to extend along its length in the first direction. The element 168 is midway between the edges of the cathode 141 in the second direction. The potential of the element 168 relative to the wafer 100 is less than the potential of the cathode 141 so that the current density of the beam B increases from the center to the edges and creates the temperature gradient shown in Fig. 8.

Fig. 17 shows an arrangement using two cathodes 141_1 and 141_2. By providing an angle A between the cathodes, the current density of the beam B can be controlled to provide the temperature gradient shown in Fig. 8.

Fig. 18 shows a modified cathode 141′. The cathode 141′ has a curved emitting surface 170 which creates a beam B having a current density at the substrate that creates a temperature gradient like that shown in Fig. 8.

Fig. 19 shows the cathode 141 heated internally by two filaments 172 and 174. The use of two spaced-apart filaments creates a current density gradient in the electron beam B which creates a temperature temperature in the region 106 like that shown in Fig. 8.

Fig. 20 shows a slight modification of the embodiment shown in Fig. 19. The cathode 141 in this embodiment comprises two cathode elements 141A and 141B which have the filaments 172 and 174 embedded therein, respectively. The cathode elements 141A and 141B are separated by an insulating member 176. When the filaments 172 and 174 are heated by the passage of current therethrough, the cathode elements 141A and 141B create a beam B the current density of which at the wafer surface establishes the temperature distribution shown in Fig. 8.

In the embodiment of Fig. 21, the cathode 141 is coated with two areas 178 of material, for example, Ba_2O with cesium, having a higher emissivity of electrons than the material of the cathode 141. When the cathode 141 is heated the areas 178 emit more electrons and create the temperature distribution shown in Fig. 8.

Of course, to create both temperature gradients shown in Figs. 6 and 8, any of the embodiments in Figs. 12–15 can be combined with any of the embodiments in Figs. 16–21. For example, the cathode shown in Fig. 21 could be heated along its length as shown in Fig. 12 to create the longitudinal and lateral temperature gradients shown in Figs. 6 and 8, respectively.

It is also possible initially to create a uniform temperature in the region 106 and control the manner in which it cools non-uniformly to provide solidification in the proper directions as described above in connection with Figs. 7 and 9.

Figs. 22–24 illustrate a wafer provided with a structure that creates the temperature gradient over time shown in Fig. 7 as the region 106 cools. The substrate includes a thermal layer 200 on which is provided the region 106 of polysilicon. The thermal layer 200 provides different rates of heat conduction in different areas thereof. The thermal layer 200 comprises a first layer 202 of a good heat conductor such as polysilicon deposited by any well-known method such as CVD. On top of the first layer 202 a second layer 203 of a heat-insulating material such as SiO_2 is formed by CVD. The second layer 203 is masked and etched by well-known techniques to form a fence 204 that defines the region 106. At one end of the region 106 a portion 206 of the second layer 203 is etched to a slightly greater depth than the remainder of the region 106. Polysilicon is then deposited in the region 106 bounded by the fence 204.

When the substrate 102 shown in Figs. 22–24 is subjected to the electron beam, it is initially heated throughout, say to an even temperature as shown in Fig. 7. However, as it cools the portion 206 forms a heat sink because of the reduced thickness of the second layer of heat-insulating material 203. Furthermore, the fence 204 retards heat flow from the molten polysilicon in the region 106 in directions other than through the portion 206. Thus, the region 106 cools as shown in Fig. 7 and solidifies in the direction of the arrow 108 shown in Fig. 5.

In an alternate embodiment, the second layer 203 is changed slightly as shown in Fig. 25. In this embodiment, the thickness of the layer 203A gradually increases from one end of the region 106 to the other. When the region 106 of polysilicon is exposed to a uniform electron beam, it melts and then solidifies again as shown in Figs. 5 and 7.

In still another embodiment, as shown in Fig. 26, the second layer 203 is substantially as shown in Fig. 24. However, the effect of the heat sink action of the portion 206 is enhanced by providing a heat-conducting radiator 210 in contact with the polysilicon in the region 206. The radiator 210 conducts heat from the end of the zone 208 and radiates it into the ambient surroundings to enhance the cooling pattern provided by the wafer shown in Fig. 24.

It is also possible to enhance the cooling pattern described in connection with Fig. 7 by preventing exposure of certain parts of the zone to the electron beam B. As shown in Fig. 27, a substrate 102 is provided with the

layers 202 and 203 substantially as shown in Fig. 24. A mask 212 is disposed above the heat sink formed by the reduced-thickness portion 206 to prevent the extreme end of the region 106 from being exposed to the electron beam B. Thus, a relatively cooler region is provided which enhances the heat flow and provides the cooling pattern illustrated in Fig. 7.

Fig. 28 shows a slight modification of the embodiment shown in Fig. 27, in which a mask is also used as a radiator, similar to the radiator 210 shown in Fig. 26. In Fig. 28 the radiator 212′ masks some of the polysilicon in the region 106 from exposure to electrons. In addition, because it is in contact with the polysilicon in the region 106, it also acts as a radiator further to enhance the required cooling pattern.

It is also possible to construct a wafer that controls the manner in which the region cools laterally (in the second or x-direction) as described above in connection with Fig. 9. Figs. 29–31 describe in detail such a wafer construction.

In Fig. 29 the substrate 102 includes a thermal layer 200 deposited on the base of the substrate and comprising a first layer 202′ of a heat-conducting material and a second layer 203′ of a heat-insulting material. As described above in connection with Figs. 24–26, the layer 202′ will typically consist of polysilicon. After deposition that layer is etched to form a small ridge 214 running in the y-direction as shown in Fig. 29. On top of the first layer 202′ of polysilicon, the second layer 203′ of heat-insulating material, such as SiO_2, is formed and then etched to provide the cross-section shown in Fig. 29. More particularly, the second layer 203′ is etched to provide the fence 204 around the region 106 and a central portion 216 overlying the ridge 214 and having a reduced thickness. The layer of polysilicon which will form the seed crystal is deposited in the region 106. The substrate 102 is then subjected to a uniform electron beam which heats it above its melting point. As the molten polysilicon in the region 106 cools, a temperature gradient is established as described in connection with Fig. 9, so that the direction of solidification proceeds as shown in Fig. 5. The reduced thickness portion of the layer 203′ in the middle of the region 106 acts as a heat sink to establish the proper temperature gradient in the cooling polysilicon.

In Fig. 30, a slightly altered embodiment of the configuration shown in Fig. 29 is illustrated. In constructing the wafer shown in Fig. 30, the step of etching the first layer 202′ of polysilicon is omitted. Thus, a uniform layer 202 of polysilicon, like that shown in Figs. 24–26, is disposed on the substrate 102 beneath the etched layer 203′ of SiO_2. When the region 106 of polysilicon is melted by the uniform electron beam, the reduced thickness area 216′ in the center of the region 106 acts as a heat sink, like that described in connection with Fig. 29.

In Fig. 31 another embodiment is shown. The substrate 102 and the first layer 202 are substantially identical to those described in connection with Fig. 30. However, the layer of insulting material is etched to provide a second layer 203″ with the cross-section shown in Fig. 31. Thus, when the region 106 is subjected to a uniform electrical beam, and initially heated as shown in Fig. 9, it will cool and solidify as shown in Fig. 5.

Figs. 32 and 33 show another embodiment for establishing the cooling patterns shown in Fig. 5. A substrate 102 is provided with the thermal layer 200 comprising a first layer 202 of polysilicon and a second layer 203 of SiO_2 substantially as has already been described. Within the fence 204 a heating member 218, made of a material which absorbs electrons and is heated thereby, surrounds the periphery of the region 106. This member 218 typically is made of a material with properties such that the parameter $k\rho C$ (where k = thermal conductivity in watts/cm-°C, ρ = density in g/cm^3 and C = specific heat in Joules/ g-°C), is relatively low, say below 1.0, which is value of $k\rho c$ for silicon. A typical example of such a material is titanium, which has a value of $k\rho C = 0.2$. Qualitatively, the parameter $k\rho C$ can be regarded as a measure of how readily a material will heat when exposed to energy, with materials which heat more readily exhibiting smaller values for $k\rho C$. When the region 106 is subjected to the electron beam, the heating member 218 is heated and the heat thereof is retained because of the insulating characteristics of the fence 204. Thus, the cooling pattern shown in Fig. 5 is further enhanced.

Thus, a single crystal can be formed on a relatively inexpensive substrate material. Those skilled in the art will recognize that the embodiments thus far disclosed can be used in almost any combination to provide the solidification pattern shown in Fig. 5. For example, an electron beam which creates an initial temperature gradient could be used with a wafer configuration which enhances solidification in the necessary directions. Or the wafer construction can be used to create a cooling pattern in one direction while the apparatus used to provide the electron beam alone creates the necessary cooling pattern in the other direction.

The single crystal thus formed is particularly adapted to be used as a seed for making a large, single-crystal semiconductor device by scanning with the strip-like electron beam B as shown in United States Patent Application Serial No. 492,800, filed May 9, 1983, and assigned to the assignee of the present invention. Thus, it is particularly convenient to use

the same type of electron beam to melt the region 106, which results in an elongated rectangular seed, as shown herein. However, those skilled in the art will recognize that other seed-crystal shapes are possible.

After a seed has been formed, the same or a similar electron beam is used to scan the wafer to form a large, single-crystal semiconductor device in accordance with the disclosure in the aforementioned patent application. In particular, Fig. 34 shows schematically the use of the electron beam B to scan the surface of the wafer 100. The beam B begins at a location such that it melts some but not all of the single-crystal seed in the region 106 and then is moved relative to the wafer 100 to create a molten zone in a polysilicon layer on the substrate which grows into a single crystal from the seed. As shown in Fig. 34, the portion 114 of the seed is not usable and generally is etched off the substrate before it is scanned by the electron beam to create the semiconductor device.

Figs. 35–38 illustrate in detail how the seed can be used to create a large, single-crystal semiconductor device.

Fig. 35 shows a wafer 100 having a cross-section similar to that shown Fig. 30. The layer 220 of polysilicon which is used to form the seed is generally deposited over the entire surface of the subtrate prior to creating the seed, a detail which was omitted from the description above for the sake of clarity. That approach saves the manufacturing expense and time which would be required to mask those areas of the surface of the substrate which were not going to be used to form the seed. In any case, Fig. 35 shows the wafer 100 after the seed has been formed in the region 106.

Fig. 36 shows a chemical-resist mask 300 which is deposited over the surface of the wafer and then etched to expose one side of the fence 204 and the portion of the layer 220 of the polysilicon which was not formed into the seed by the electron beam B. In Fig. 37, the wafer 100 is shown after the layer 220 of polysilicon and one side of the fence 204 has been removed by etching and after the chemical-resist mask 300 has been removed. An operating layer of polysilicon 302 is then deposited partially on the seed as shown in Fig. 38 by conventional techniques. The wafer 100 in Fig. 38 can then be scanned by the electron beam B as illustrated in Fig. 34 to form a large single-crystal semiconductor device by lateral epitaxial recrystallization of the operating layer.

Fig. 39 illustrates a wafer configuration that enhances the tendency of the molten polysilicon, created when the layer 302 is scanned by the electron beam B, to solidify in the proper direction.

As discussed in Patent Application Serial No. 492,800, the direction of solidification of the molten polysilicon must be controlled if a good quality, single-crystal layer is to be provided. Specifically, solidification should proceed in the same direction for the entire region in which the single crystal is to be provided. The construction shown in Figs. 35–38 conveniently provides for enhancing the tendency of the polysilicon to solidify in the same direction because of the heat sink provided to form the crystal. By using the same techniques in forming the large single-crystal device that were used in forming the seed, that tendency can be further enhanced.

As shown in Fig. 39, the wafer 100 shown in Fig. 38 can be prepared with a fence 204 of SiO_2 around the layer 302 polysilicon that will form the single crystal when scanned by the electron beam B. (Depiction of the edges of the seed S and the layer 302, which are shown in Fig. 38, has been omitted from Fig. 39 for clarity.) The reduced thickness portion 216' will thus provide a heat sink while the fence 204' retards heat flow from the remainer of the region.

Those skilled in the art will recognize that any of the configurations shown in Figs. 29–31 will provide a heat sink when the layer 302 of polysilicon is scanned to produce a large single-crystal. In addition, the use of a heating member like that shown in Figs. 32–33 can also be used to provide the desired direction of heat flow in the molten polysilicon area.

Those skilled in the art will realize that it might be desirable to provide more than one seeding location in the path of the electron beam B as it scans the wafer surface. It will be readily recognized that it is possible to provide as many such seeds across the wafer surface as are deemed necessary and provide them with the proper spacing as well. For example, the cross-section shown in Figs. 29–31 can be repeated as many times as are desired on the surface of the substrate to provide multiple seeding locations on the wafer shown in Figs. 34–38.

Thus a large, single-crystal semiconductor device can be provided on a relatively inexpensive substrate material because the substrate is not the source of the seed, as in the technique described in Patent Application Serial No. 492,800. In addition, because the depth of the molten zone can be precisely controlled using the electron beam disclosed herein, it is possible to create a seed in only the upper portion of the polysilicon layer on the substrate and then also to form a single crystal in only an upper portion of the polysilicon layer. Using that technique, a single-crystal device can be created directly on top of a layer of polysilicon.

Fig. 40 illustrates the use of the electron beam B to scan a substrate to form a plurality of seeds S. For example, assume that the wafer 100 was provided with a plurality of

regions 106 having the cross-section shown in either Fig. 29, 30 or 31. The electron beam B is then used to scan the wafer as shown in Fig. 40. The proper direction of solidification in the first direction is established by the scanning beam as discussed in Patent Application Serial No. 492,800. The temperature distribution in the second direction, across the region 106, is estabished as discussed above in connection with Figs. 29–31. Thus, a plurality of seeds S can be formed in one continuous process.

In a variation on this embodiment, shown in Figs. 41 and 42, the electron beam intensity is varied along the length or width of the cathode, respectively. The wafer 100 with a single uniform layer of polysilicon, as shown in Fig. 2 for example, is scanned using such an electron beam B. A plurality of alternating hot and cool zones are formed on the surface of the substrate as shown in Fig. 43. The resulting solidification pattern corresponds to that shown in Fig. 5 and thus a plurality of seeds can be formed without using the various configurations of fences, heat sinks and masks discussed above. Of course the temperature profile shown in Fig. 41 can be repeated many times across the width of the cathode to form a plurality of seeds as the beam scans the wafer. In addition, by turning the beam on and off, a pattern of seeds like that shown in Fig. 40 can be created.

Those skilled in the art will recognize from Figs. 10–21 how to construct apparatus for providing an electron beam for providing the temperature pattern shown in Figs. 41 and 42. For example, the electron beam depicted in Fig. 42 can be provided by any of the configurations discussed above and shown in Figs. 16–21.

Fig. 44 illustrates in particular how the general principles thus described can be used to form seeds having any desired configuration. As shown in Fig. 43, the wafer 100 has a thermal layer with a cross-section similar to that shown in Fig. 24, for example. A plurality of regions 106 are provided adjacent to and spaced from each other and a common heat sink is provided in the area 206 having a reduced thickness insulating layer. As the electron beam B scans the wafer, a seed is formed in each region 106. The long dimension of the beam moves normal to the regions 106 for forming the seeds and, to produce the final device, the beam scans the wafer with its long dimension parallel to the seeds formed in the regions 106. The formation of the seeds can be enhanced by not turning on the electron beam until part of the region 206 has been traversed, which will make the region 206 even cooler and promote heat flow in the proper direction.

The advantages of the present invention will be apparent to those skilled in the art. A large, single-crystal semiconductor device or a plurality of such devices having almost any desired configuration can be easily and quickly made on virtually any substrate material. The expense both in terms of material costs and yields of large, single-crystal semiconductor devices can be significantly increased by using the present invention.

The present invention has been described by referring to many particular embodiments. However, those skilled in the art will recognize that numerous modifications other than those specifically pointed out can be made without departing from the spirit of the invention. For that reason, the scope of present invention is limited and defined solely by the following claims.

CLAIMS

1. A wafer comprising a substrate base, a thermal layer on said substrate base and a polycrystalline or amorphous seed layer or a region of said thermal layer, wherein:

said thermal layer provides different rates of heat conduction therethrough in at least one of a first direction of said region and a second direction of said region substantially normal to said first direction;

said different rates of heat conduction are provided through said thermal layer in said first direction for creating an increasing temperature gradient in said seed layer in said first direction; and

said different rates of heat conduction are provided through said thermal layer in said second direction for creating a higher temperature at the edges of said region than centrally thereof in said second direction.

2. A wafer as in claim 1; wherein:

said thermal layer includes a first layer of heat-conducting material on said substrate base and a second layer of heat-insulating material on said first layer; and

said second layer includes a fence surrounding said region of said seed layer and a portion underlying said region and having different thicknesses in different parts of said region.

3. A wafer as in claim 2; wherein said thermal layer varies said rate of heat conduction in said first direction.

4. A wafer as in claim 3; wherein said underlying portion comprises a first are a having a substantially uniform thickness in said first direction and a second area at one end of said region having a reduced thickness relative to said first area.

5. A wafer as in claim 3; wherein said underlying portion gradually increases in thickness in said first direction.

6. A wafer as in claim 2; further comprising a heat-radiating member in contact with said seed layer.

7. A wafer as in claim 6; wherein said heat-radiating member is disposed proximate to an end of said region in said first direction.

8. A wafer as in claim 7; wherein said heat-radiating member is embedded in said seed layer.

9. A wafer as in claim 2; wherein said thermal layer varies said rate of heat conduction in said second direction.

10. A wafer as in claim 9; wherein said underlying portion comprises a heat-sink area substantially centrally located in said region in said second direction and having a reduced thickness relative to the remainder of said portion viewed in a plane in said second direction.

11. A wafer as in claim 10; wherein said heat-sink area and said remainder have substantially uniform thicknesses.

12. A wafer as in claim 11; wherein said second layer has an increased thickness underlying said heat-sink area.

13. A wafer as in claim 12; wherein said portion has a first thickness substantially in the center thereof in said second direction and gradually increases in thickness toward the edges thereof in said second direction.

14. A wafer as in claim 2; further comprising a heating member disposed between said fence and said seed layer, said heating member comprising a material for which the parameter $k\rho C$ (where k is thermal conductivity in watts per cm-sec, δ is density in grams per cm^3 and C is specific heat in Joules per gram-°C) is less than 1.0.

15. A wafer as in claim 14; wherein said heating member comprises a material for which the parameter k C is about 0.2.

16. A wafer as in claim 15; wherein said heating member is titanium.

17. A wafer as in claim 16; wherein said first layer is polysilicon, said second layer is silicon dioxide and said seed layer is polysilicon.

18. A wafer as in claim 2; wherein said heat-insulating material is selected from the group consisting of silicon dioxide and silicon nitride.

19. A wafer as in claim 18; wherein said heat-insulating material is silicon dioxide.

20. A wafer as in claim 1; wherein said polycrystalline or amorphous layer is polysilicon.

21. A wafer as in claim 1; wherein said substrate base comprises a material selected from the group consisting of glass, quartz, sapphire and crystalline silicon, germanium and gallium arsenide.

22. A wafer as in claim 21; wherein said substrate base comprises a single-crystal semiconductor material having a semiconductor-device region therein and said thermal layer comprises an electrically insulating material.

23. A wafer as in claim 1; wherein said polycrystalline or amorphous operating layer is between 0.5 and 1.0 micron thick.

24. A wafer as in claim 1; wherein:

said thermal layer includes a first layer of heat-conducting material on said substrate base and a second layer of heat-insulting material on said first layer;

said substrate includes a plurality of said regions having at one end thereof in said first direction a common area underlain by a portion of said second layer having a thickness less than the thickness of the remainder of said second layer; and

said second layer includes a fence substantially surrounding said regions and said common area.

25. A wafer comprising a substrate base, a thermal layer on said substrate base, substantially a single crystal seed on said thermal layer extending in a first direction and a polycrystalline or amorphous operating layer on said thermal layer covering an area bounded on one side by said seed and extending in a second direction away from said seed and normal to said first direction; wherein:

said polycrystalline or amorphous operating layer is in contact with said seed; and

said thermal layer provides different rates of heat conduction through said thermal layer in said second direction for creating an increasing temperature gradient in said operating layer in said second direction.

26. A wafer as in claim 25; wherein:

said thermal layer includes a first layer of heat-conducting material on said substrate base and a second layer of heat-insulating material on said first layer; and

said second layer includes a fence surrounding at least a portion of the boundary of said polycrystalline or amorphous operating layer other than the portion of said boundary in contact with said seed and a reduced thickness portion proximate to said seed.

27. A wafer as in claim 26; wherein said reduced thickness portion underlies said seed and the remainder of said second layer has a uniform thickness.

28. A wafer as in claim 25; wherein said substrate base comprises a material selected from the group consisting of glass, quartz, sapphire and crystalline silicon, germanium and gallium arsenide.

29. A wafer as in claim 28; wherein said first layer is polysilicon, said second layer is silicon dioxide, said seed is silicon and said operating layer is polysilicon.

30. A wafer substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

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